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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,665	10/06/2000	Avner Dor	10559-346001 / P8300	9766

20985 7590 07/16/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/680,665	DOR ET AL.
	Examiner	Art Unit
	Chat C. Do	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 16-24* is/are pending in the application.

4a) Of the above claim(s) *1-8 and 16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13 and 21,24* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/29/04*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *attached* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 04/29/2004.

2. Claims 13 and 16-24 are pending in the application. Claims 1, 9, 16, and 21 are independent claims. In Amendment, claims 14-15 are cancelled and claims 16-24 are added. This action is made non-final after a RCE filed 04/29/2004.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8 and 16-20, drawn to a method of transforming matrix, classified in class 708, subclass 607.

II. Claims 9-13 and 21-24, drawn to apparatus comprising general hardware component for multiplying and adding, classified in class 708, subclass 523.

The inventions are distinct, each from the other because of the following reasons:

4. Inventions of Group I and Group II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, for instance a method of processing digital signal data by arranging and transforming as cited in Group I can be done purely by hand, or (2) the apparatus as claimed can be used to practice another and materially different process, for instance an apparatus for performing digital signal data comprising basis hardware components as cited in Group II can be used to perform other functions such as processing FFT or IFFT as seen in Nakai et al.

(U.S. 6,115,728). (MPEP § 806.05(e)). In this case, the process as claimed can be practiced by hand such as a method of processing digital signal data by arranging and transforming can be done purely by hand without particular need of particular hardware structure as Group I discloses a method of transforming or processing matrices and Group II discloses a general apparatus comprising hardware component for performing multiplication and addition.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with William E. Hunter on 07/07/2004 a provisional election was made without traverse to prosecute the invention of Group II, claims 9-13 and 21-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims of Group II, 1-8 and 16-20, withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Information Disclosure Statement

9. The information disclosure statement filed 04/29/2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the applicant fails to provide a complete copy of the listed reference with designated ID "AQ". The applicant only provides a table of content of this reference. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

11. Claims 9-13, 21, and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Nakai et al. (U.S. 6,115,728).

Re claim 9, Nakai et al. disclose in Figure 1 an apparatus for performing a linear transformation (e.g. abstract wherein the linear transform is FFT) comprising: first and second inputs (e.g. first input into 101 and 104 for

coefficients) which receive input data (e.g. as data) and predetermined data (e.g. as coefficients); transformation circuitry (103) which acts on the input data and predetermined data; control and address generation circuitry (105) connected to a first memory (RAM #0), which generates corresponding addresses for accessing cells memory, and for controlling the selection between a data receiving mode, in which data is received via first input, and a data processing mode, in which the arrival of incoming data via first input is blocked; and counter circuitry (e.g. output of 106) for controlling the timing of the operations of the apparatus; wherein the control and address generation circuitry comprises: a second memory (RAM #1) which stores pre-programmed processing and control data; a comparator circuitry (e.g. output of control circuit unit which uses to control the mux(es) in 121) which switches between the data receiving mode and the data processing mode; a first set of multiplexers (121), each of which having at least one direct input for receiving transformation data, and another input, into which transformation data is fed via a corresponding inverter, first set being controlled to transfer transformation data or, inverted transformation data, by a predetermined value provided by transformation data; a second set of multiplexers (122), each of which having at least one input connected to the output of a corresponding multiplexer selected from first set of multiplexers, and another input, connected to second memory, second set being controlled by comparator circuitry (e.g. output of control unit to 122) to provide a first address to the first memory by transferring the output of each multiplexer from first set to the output of its corresponding multiplexer from second set or, to provide at least a portion

of the second address to the first memory by transferring data stored in second memory; and a multiplexer (122), operating in combination with second set of multiplexers in data processing mode, having an unconnected input and an input connected to second memory and controlled by comparator circuitry, thereby providing the remaining portion of second address (105).

Re claim 10, Nakai et al. further disclose in Figure 1 the transformation circuitry (103 as butterfly operation) multiplies each element of the input data by a corresponding element of the transformation data.

Re claim 11, Nakai et al. further disclose in Figure 1 the transformation circuitry comprises a memory which stores the result of the multiplication (e.g. internally in 103 as seen in Figure 4 and externally to output port of 121).

Re claim 12, Nakai et al. further disclose in Figure 1 the transformation circuitry comprises summation and accumulation circuitry (Figure 5 e.g. X0 = x0+x1+x2+x3).

Re claim 13, Nakai et al. further disclose in Figure 1 a multiplexer circuitry which selects between the data receiving mode and the data processing mode (e.g. 121).

Re claim 21, it has similar limitation cited in claim 12. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 24, it has same limitation cited in claim 13. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Allowable Subject Matter

12. Claims 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

13. Applicant's arguments with respect to claims 9-13 and 21-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,138,730 to Ali discloses a high speed FFT processor.

b. U.S. Patent No. 5,481,487 to Jang et al. disclose a transpose memory for DCT/IDCT circuit.

c. U.S. Patent No. 6,185,595 to Hori et al. disclose a discrete cosine transformation operation circuit.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

July 12, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100